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Design and Analysis of an Array Multiplier Using an Area Efficient Full Adder Cell in 32nm CMOS Technology

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----------Abstract----------
Multiplier is one of the basic functional unit in digital signal processor. Most high performance DSP systems rely on hardware multiplication to achieve high data throughput. In this paper a low power and low area array multiplier is proposed. The conventional array multiplier is synthesised using 16T full adder cell. In conventional array multiplier the final stage of addition is removed and the carry bits are given to the input of the next left column input, thereby causing a large trade off in power and area. The proposed array multiplier is synthesised using 10T full adder cell. The proposed array multiplier design uses 96 less transistor count and saves 2.82% of total power, 13.24% of more speed and 15.69% less power delay product when being compared with the conventional array multiplier in 32nm MOSFET Technology using HSPICE.

Keywords*- array multiplier, full adder, low power, VLSI.*

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1. Introduction

In today's world low power issues have become an major important factor in modern VLSI design. In fact, Low Power VLSI chips have emerged as highly in demand for designing any subsystem. Low power circuit is realized using both hardware and software approach.[12] The limited power capacity of the portable system has lead designers to more power aware designs. Energy efficient circuits are required because of the increasingly stringent demands for battery space and weight in portable multimedia devices, particularly in digital multipliers which are basic building blocks of digital signal processors. Besides adders, digital multipliers are the most critical arithmetic functional unit in many DSP applications such as in filters, Fourier transform and discrete cosine transform and in multiplier accumulate unit. Both array and parallel multipliers are in high demand because of their high execution speed and throughput. [5] The advantage of array multiplier is its regular structure; therefore layout becomes simple and it occupies less area since it has small size. In VLSI, the regular structures can be cemented one over another; this reduces the amount of mistakes and also reduces layout design. A basic multiplier can be divided into three parts partial product generation ,partial product addition and final addition .In this paper we present a low power ,low area design methodology for parallel array multiplier using carry save adder. Power dissipation is the most important parameter for portability & mobility and it is classified into dynamic and static power dissipation. Dynamic power dissipation arises when the circuit is overall consuming that means when its operational, while static power dissipation arises when the circuit is inactive or is in a power down mode. There are three main components of power consumption in digital CMOS VLSI circuits [8].

1) Switching Power: arises because of the charging and discharging of the circuit capacitances during transistor switching.
2) Short Circuit Power: arises due to short circuit current flowing from power supply to ground during transistor switching.
3) Static Power: arises when the circuit is in stable state due to static and leakage currents flowing. The first two are referred to as dynamic power as the power is consumed dynamically while the circuit is changing states.[8]

In designing a low power CMOS 1 bit full adder, the emphasis will on the following areas [10].

[1] To reduce the total number of transistor count in the design and to reduce the load capacitance also to reduce the total number of parasitic capacitances in internal nodes
[2] To save the dynamic power consumption by lowering the switching activity.

[3] To remove some direct paths from the power supply to ground to save the short circuit power dissipation.
[4] To reduce the appearance of glitches which leads to unnecessary power dissipation also leads to fault circuit operation due to spurious transitions especially in low voltage operation system.
[5] In order to build a low power full adder, all the internal nodes in the circuit must possess full voltage swing at the output nodes.
[6] To build the low voltage full adder design because the power supply voltage is the crucial factor in reducing power dissipation.[8]

In order to reduce the power consumption of the adders any one of the above factors of the circuit need to be reduced. In nanometer scale leakage power dominates the dynamic power and static power due to hot electrons. So the concentration is on trade off power in array multipliers.

II. Conventional Array Multiplier

An existing array multiplier is very much regular in its structure when compared to the conventional array multiplier and uses an only short wire that goes from one full adder cell to adjacent full adder cell. It has very simple and efficient layout in VLSI and can be easily and efficiently pipelined.The conventional array multiplier is synthesised using 16T full adder cell. The existing full adder cell is made of 16T which is designed using XNOR gate, pass transistor and transmission gate . The 16T full adder cell consumes less power when compared to the conventional CMOS full adder cell that uses 28 transistor. This cell produces full swing at the output nodes. This low power full adder cell has a drawback of giving large delay when compared to other adders. This circuit can operate with full output voltage swing but consumes significant amount of power and have more delay compared to other adders having less transistor count. The existing array multiplier is synthesized using 16T full adder cell [2].Consider the multiplication of two unsigned n-bit numbers, where X = Xn-1, Xn-2, ... Xo is the multiplicand and Y =Yn-1,Yn-2..... Y0 is the multiplier. The product of these two bits can be written as P7P6P5P4P3P2P1P0.Where P0 is the LSB AND P7 is the MSB.Fig1.shows multiplication of a 4*4array multiplier using carry save adders.[1]

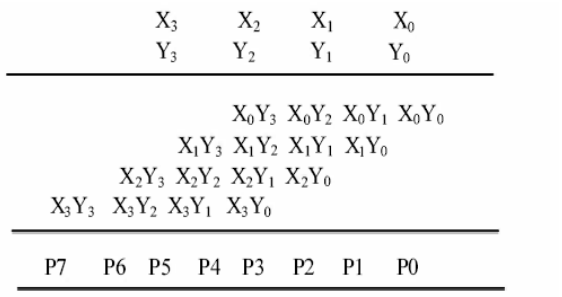

FIG1. 4*4 MULTIPLICATIONS [1]

The conventional array multiplier uses carry save addition to add the products.[1]In the carry save addition method, the first row will be either half adders or full adders .If the first row of the partial products is implemented with full adders ,Cin will be considered '0'.Then the carries of each full adder can be diagonally forwarded to the next row of the adder. The resulting multiplier is said to be carry save array multiplier as the carry bits are not immediately added but rather saved for the next stage of addition. Hence the name carry save multiplier. In the design if the full adders have two input data the third input is considered as zero. The final adder which is used to add carries and sums of the multiplier is removed. Then the carries of the multiplier at the final stage is carefully added to the inputs of the multiplier as shown in Fig2.The carry of the fourth column of the multiplier is given to the input of the fifth column instead of zero. Then the carry of the fifth column is forwarded to the input of the sixth column so on. And in this carry of the seventh column of the adder is considered as the most significant bit of the multiplier. In this paper conventional array multiplier is synthesised using 16T full adder cell.[2]

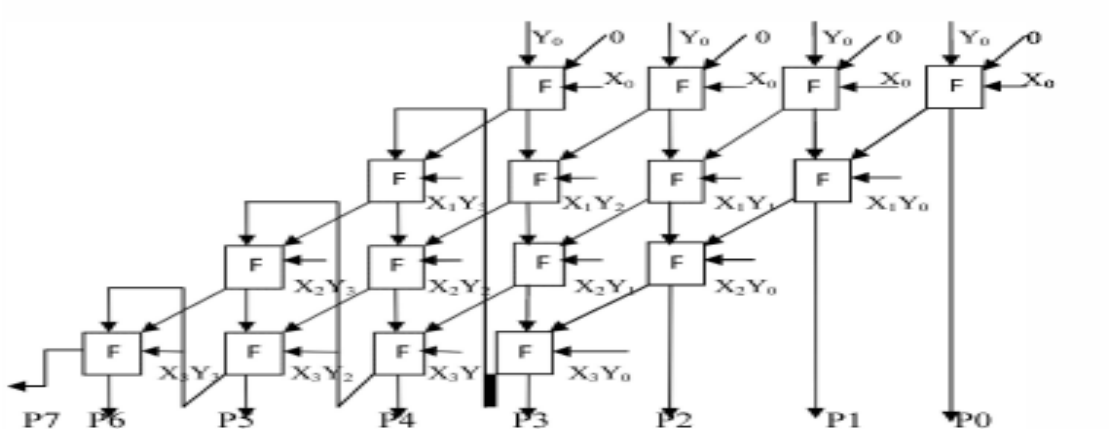

FIG2. ARRAY MULTIPLIER USING CSA [1]

III. Proposed Array Multiplier

In the proposed array multiplier the full adder cells is implemented using 10T full adder cell as shown in Fig3. The 10T full adder circuit is designed using inverted based 4T XOR gates in the designed full adder cell and shows remarkable improvements in power and delay. [3]This 1 bit full adder cell has less power consumption as it has no direct path to ground .The elimination of a path to the ground reduces power consumption .It is observed that the newly designed 10-T adder has no direct path to the ground. The charge stored at the load capacitance is reapplied to the control gates. The circuit produces full-swing at the output nodes. The circuit even fails to provide so for the internal nodes. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design. Due to multiple threshold problems it cannot be cascaded at low power supply. Also the circuit becomes slower as the power consumption by the circuit reduces. Thus implementing the array multiplier using 10T full adder cell shows to be more power and area efficient when compared with the 16T full adder cell .

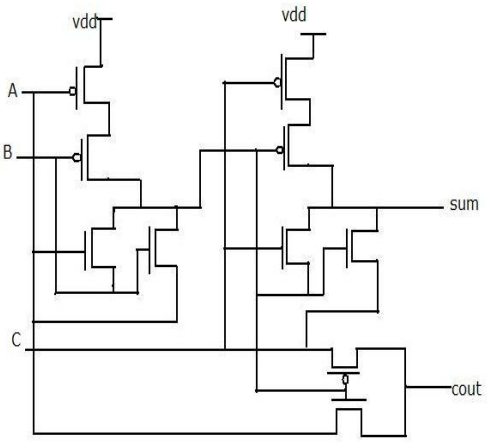

FIG3.10T FULL ADDER CELL [3]

IV. RESULT AND DISCUSSION

The 16T and 10T full adder cell is analysed in terms of power, propagation delay and power delay product in both 32nm & 130nm MOSFET technology using H-spice. The conventional array multiplier designed using 16T full adder cell is compared with the proposed array multiplier designed using 10T full adder cell. Power, propagation delay and power delay product are calculated for both conventional and proposed array multiplier in both 32nm &130nm MOSFET technology using H-spice. And the transient analysis for full adders & multipliers are shown respectively.

SIMULATION OUTPUTS:SIMULATION RESULTS DESIGNED IN 32nm MOSFET TECHNOLOGY WITH OPERATING VOLTAGE OF 0.9V.

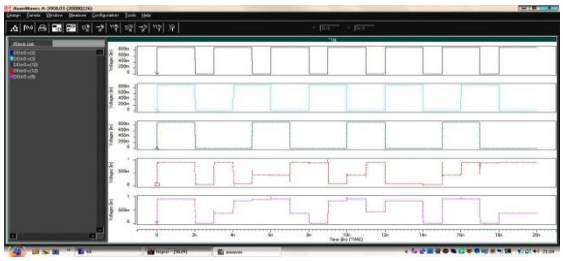

FIG4. TRANSIENT ANALYSIS OF 16T FULL ADDER.

The first three (a, b, c) are the inputs to the full adder and the third and fourth are the sum and carry respectively of a 16T full adder cell.

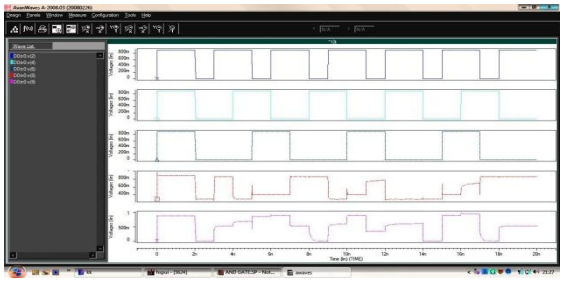

FIG5. TRANSIENT ANALYSIS OF 10T FULL ADDER

The first three (a, b, c) are the inputs to the full adder and the third and fourth are the sum and carry respectively of a 10T full adder cell.

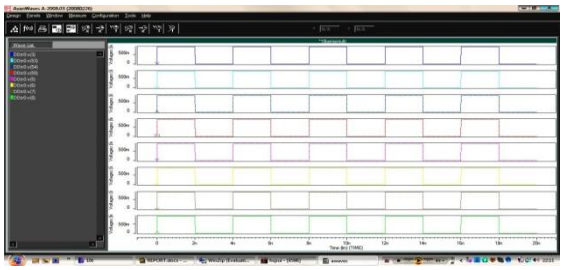

FIG: 6: TRANSIENT ANALYSIS OF EXISTING ARRAY MULTIPLIER SHOWING INPUTS.

v(3),v(53),V(54),v(55),v(5),v(6),(7),v(8) are the inputs to the existing array multiplier.

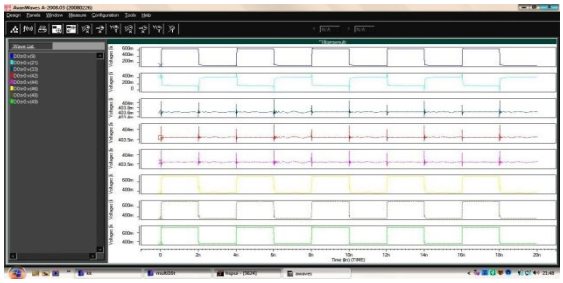

FIG:7: TRANSIENT ANALYSIS OF EXISTING ARRAY MULTIPLIER SHOWING OUTPUTS .

v(9),v(21),v(33),v(42),v(46),V(48),v(49) are the outputs of the existing array multiplier.

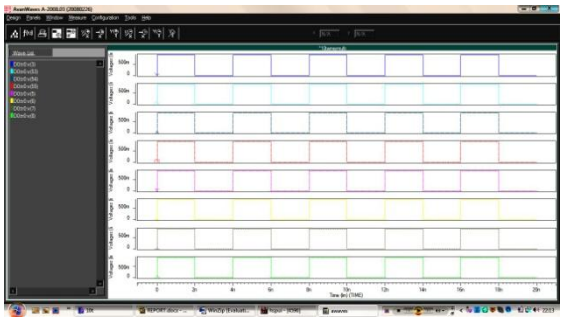

FIG: 8: TRANSIENT ANALYSIS OF PROPOSED ARRAY MULTIPLIER SHOWING INPUTS.

v(3),v(53),V(54),v(55),v(5),v(6),(7),v(8) are the inputs to the proposed array multiplier.

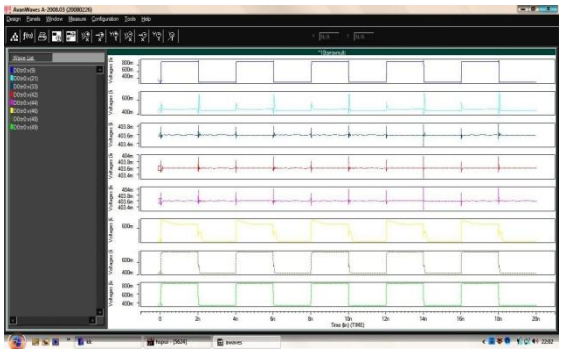

FIG: 9: TRANSIENT ANALYSIS OF PROPOSED ARRAY MULTIPLIER SHOWING OUTPUTS.

v(9),v(21),v(33),v(42),v(46),V(48),v(49) are the outputs of the proposed array multiplier.

ANALYSIS OF FULL ADDERS:

Table1. Analysis of full adder cell in 130nm technology.

FULL ADDER	POWER(W)	DELAY(S)	PDP(J)
EXISTING	5.986e-05	4.67e-12	27.95e-17
PROPOSED	4.049e-05	4.03e-12	16.48e-17

Table2. Analysis of full adder cell in 32nm technology.

FULL ADDER	POWER(W)	DELAY(S)	PDP(J)
EXISTING	2.681e-05	4.76e-12	12.76e-17
PROPOSED	1.874e-05	3.99e-12	7.47e-12

ANALYSIS OF ARRAY MULTIPLIERS:

Table3. Analysis of array multiplier in 130nm technology

ARRAY MULTIPLIER	POWER(W)	DELAY(S)	PDP(J)
EXISTING	5.77e-04	4.32e-10	24.93e-14
PROPOSED	4.36e-04	1.95e-10	8.50e-14

Table4. Analysis of array multiplier in 32nm technology

ARRAY MULTIPLIER	POWER(W)	DELAY(S)	PDP(J)
EXISTING	4.45-04	5.74e-11	25.58e-15
PROPOSED	4.33e-04	4.98e-11	21.56e-15

Table 5: Comparison of power dissipation for proposed full adder among various technologies

TECHNOLOGY	POWER(W)
MOSFET(130nm)	4.049e-05
MOSFET(32nm)	1.874e-05

Table6: Comparison of power dissipation for proposed array multipliers among various technologies

TECHNOLOGY	POWER(W)
MOSFET(130nm)	4.361e-04
MOSFET(32nm)	4.331e-04

Table 7: Analysis of power, delay and power delay product for existing and proposed array multiplier.

Technology	Array Multiplier	Power (W)	Power (%)	Delay (S)	Delay (%)	PDP (J)	PDP (%)	Transistor count
32nm	Conventional	4.457e-04	2.82	5.74e-11	13.24	25.583e-15	15.69	256 (conventional)
	Proposed	4.331e-04		4.98e-11		21.568e-15		
130nm	Conventional	5.771e-04	24.43	4.32e-10	54.86	24.930e-14	65.89	160 (proposed)
	Proposed	4.361e-04		1.95e-10		8.503e-14		

POWER ANALYSIS:

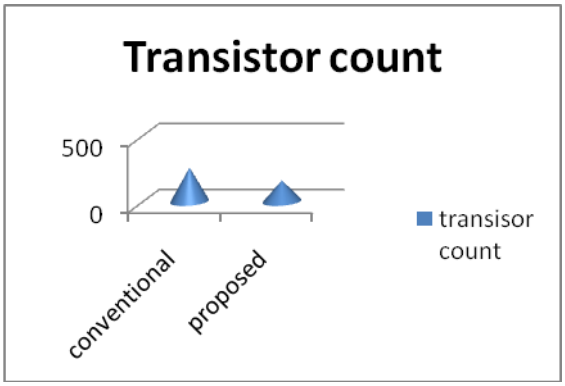

CHART 1. MULTIPLIER TRANSISTOR COUNT.

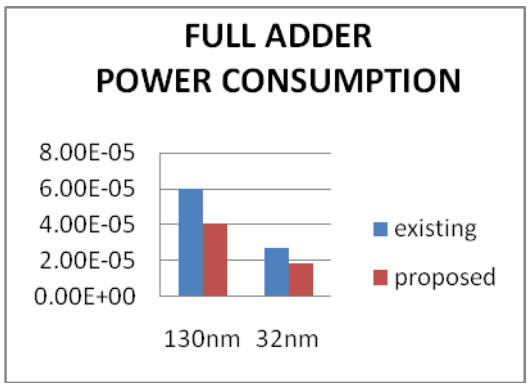

CHART 2. FULL ADDER POWER ANALYSIS.

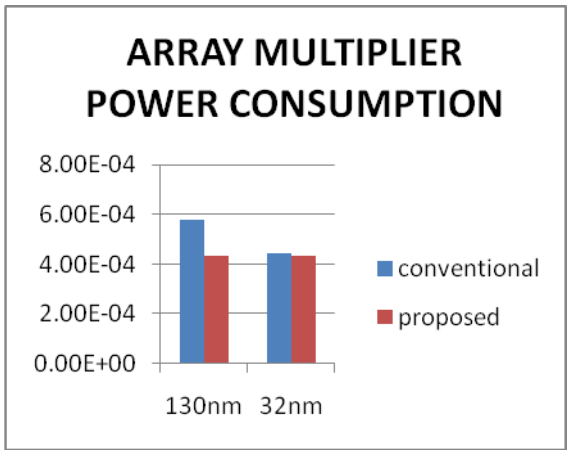

CHART 3: ARRAY MULIPLIER POWER ANALYSIS

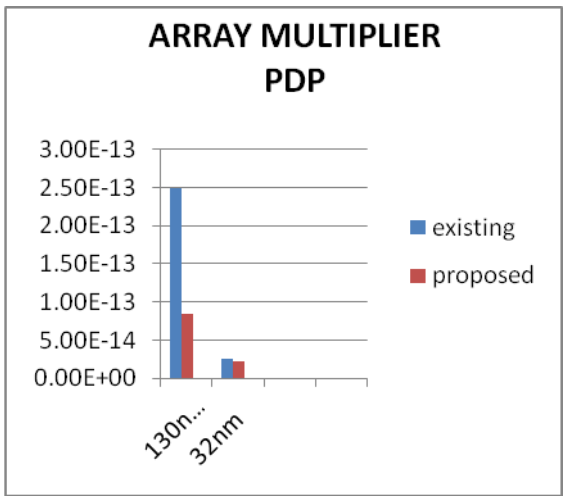

CHART4: ARRAY MULTIPLIER PDP ANALYSIS

V. Conclusion

In this paper, both the proposed and the conventional array multiplier is simulated using 32nm & 130nm MOSFET technology. The 10T full adder cell proves to be more efficient in terms of area, power and delay when compared with the 16T full adder cell. The proposed array multiplier performance increases compared with the conventional array multiplier using 16T full adder cell in terms of area, power and delay by using an area and power efficient 10T full adder cell. For 32nm MOSFET technology, the proposed design uses 96 less transistor count and saves 2.82% of total power, 13.24% of more speed and 15.69% less power delay product.

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