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Design and Analysis of a Multiplier Using an Efficient Carry Select Adder in 20nm FinFET Technology

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----------Abstract----------

A fast and energy-efficient multiplier is always needed in electronics industry especially digital signal processing, image processing and arithmetic units in microprocessor. Multipliers are such an important elements which contributes to the total power consumption of the system. Multipliers of various bit-widths are always required in VLSI from processors to application specific integrated circuits (ASICs).In this paper, design of two different array multipliers are presented, one by using Carry Select Adder using BEC logic for addition of partial product terms and another by introducing Carry Select Adder using D-latch logic in partial product lines. The multipliers described in this paper were all modelled using HSPICE for 4-bit data. The comparison is done on the basis of three performance parameters i.e. total Area, delay, Power consumption and power-delay product. To design an efficient integrated circuit considering f area, power and speed has become a challenging task in modern VLSI design field.

Keywords*- area efficient CSLA, low power, multiplier, Multiplexer and VLSI.*

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1. Introduction

As nanometer process technologies have advanced, chip density and operating frequency have increased, resulting power consumption in battery-operated devices a major factor. Even for nonportable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. This paper explores how multiplier based on FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 20-nm technology [14].

The steady miniaturization of metal-oxide-semiconductor field-effect transistors (MOSFETs) with each new generation of CMOS technology has Provided us with improved circuit performance and cost per function over several decades. However, continued transistor scaling will not be straightforward in the sub-22 nm regime because of fundamental material and process technology limits. The main challenges in this regime are twofold: (a) minimization of leakage current (subthreshold þ gate leakage), and (b) reduction in the device-to-device variability to increase yield [2]. FinFETs have been proposed as a promising alternative for addressing the challenges posed by continued scaling [14].

Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS at the nanoscale . FinFETs are double-gated transistor. The two gates of a FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. This gives rise to a rich design space.[14]Multiplication is one of the basic arithmetic operations. Most advanced digital systems today incorporate a parallel multiplication unit to carry out high-speed mathematical operations. In the past, considerable efforts were put into designing multipliers with higher speed and throughput, which resulted in fast multipliers which can operate with reduced delay time. However, the increasing importance of the power issue due to the portability and reliability concerns of electronic devices, recent work has started to look into circuit design techniques that will lower the power dissipation of multipliers [1]. Multipliers are in fact complex adder arrays.. In recent years, the growth of personal computing devices (portable computers and real time audio and video based multimedia applications) and wireless communication systems has made power dissipation a most critical design parameter [1]. In the absence of low-power design techniques applications generally suffer from

short battery life, which causes difficulties in packaging and cooling and this is leading to an unavoidable increase in the cost of the product [5]. Designing multipliers with low power, energy efficient adders reduce the power consumption and efficiency of multipliers [3].The rest of the paper is unionized as follows. Section II describes the design of a 4-bit array multiplier. In Section III the modification of carry select adder design is discussed. The result is discussed in Section IV followed by a conclusion in Section V.

II . Multiplier Design

In this section we describe the 4 bit array multiplier based on Carry Select Adder. It consists of 4 carry-select adders to obtain 8 bit output. In multiplication, multiplicand is added to itself a number of times as specified by the multiplier to generate product [5]. This is designed by shorted gate FinFETs. Shorted-gate (SG) mode of operation back gate is tied to front gate; in this case we get improved drive strength and have better control over the channel [13].

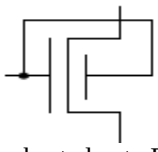

Fig.1. shorted gate FinFET

The short channel effects in double gate FET structure are well-controlled compared to single-gate devices due to control of the channel through two gates instead of one. The advantages of DG-FETs are best realized when the two gates are perfectly aligned with each other. The FinFET structure is one such successful implementation of a double-gate device. Other than the advantages in electrical performance and scalability, it also provides benefits in fabrication and manufacturability. The process flow and layout are reasonably compatible with the existing bulk CMOS process, making it more attractive for manufacturing. Owing to its superior performance and fabrication benefits, its production may start as close as the 65nm technology node. The thickness of the fin, on the other hand, defines the control of the back gate on the channel and hence the short channel behaviour of the device. Silicon films on SOI wafers are used to define the fins and hence, the height of the fin is effectively constant for all transistors [15].

2.1 Array Multiplier Design

The basic principle used for multiplication is to evaluate partial products and accumulation of shifted partial products. In order to perform this operation number of successive addition operation is required. Therefore one of the major components required to design a multiplier is Adder. In multiplication, multiplicand is added to itself a number of times as specified by the multiplier to generate product. In case of multiplier with CSLA, all partial product additions as well as final addition is carried out by using carry select logic. Figure.1 shows the schematic of a 4 bit CSLA based array multiplier. In Array multiplier, almost identical calls array is used for generation of the bit-products and accumulation. All bit-products are generated in parallel and collected through an array of adders. Array multiplier has regular structure that simplifies the wiring and the layout. Therefore, among other multiplier structures, array multiplier takes up the least area but it is also the slowest with the latency proportional to *O* (Wd) where Wd is the word length of the operand. Table 2 gives an algorithm steps and shows complete multiplication process with the help of an example. In this algorithm, S (i) represents sum of each product term, B (i) A represents each product term and P (i) represents individual bit-term of final product [11].In case of multiplier with CSLA, all partial product additions as well as final addition is carried out by using carry select logic. Fig.2 shows the schematic of a 4 bit CSLA based array multiplier.

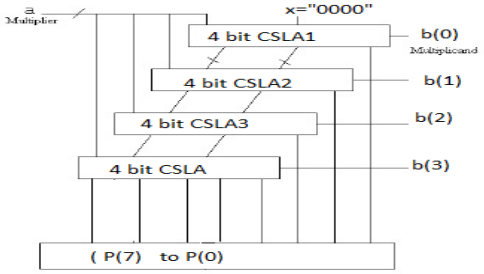

Fig.2 4-bit array multiplier using carry select adder

TABLE .1 Algorithm Steps For Multiplier Operation

A (Multiplier) B (Multiplicand)	1 0 1 0 1 0 1 1	Algorithm Steps
S(0) +B(0)A	0 0 0 0 1 0 1 0	Step 1
S(1) Shift right one bit	1 0 1 0 0 1 0 1 | 0 → P(0)	Step 2
S(1) +B(1)A	0 1 0 1 1 0 1 0	Step 3
S(2) Shift right one bit	1 1 1 1 0 1 1 1 | 1 → P(1)	Step 4
S(2) +B(2)A	0 1 1 1 0 0 0 0	Step 5
S(3) Shift right one bit	0 1 1 1 0 0 1 1 | 1 → P (2)	Step 6
S(3) +B(3)A	0 0 1 1 1 0 1 0	Step 7
S(4) Shift right one bit	1 1 0 1 0 1 1 0 | 1 → P (3)	Step 8
Final Product P (7:0)	0 1 1 0 1 1 1 0	Step 9

2.2. Carry Select Adder

It is similar to regular 16-bit SQRT CSLA. Only change is that in basic blocks having two ripple-carry adder, one ripple carry adder is always fed with 1 carry-in is replaced by BEC[4].The structure of CSLA consists of two Ripple Carry Adders, one with initial carry Cin=0 and another with carry in, Cin = 1. To replace the n-bit RCA, an n+1 bit BEC is required in order to make CSLA area and power efficient [2]. 4-bit BEC is shown in Fig.3 and Table.2. Fig.2 shows the basic function of the CSLA. One input for 8:4 mux is BEC output and the other input for the mux is the RCA with Cin=0. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal. The Boolean expressions of the 4-bit BEC are shown below

X0 = ~B0 (1)

X1 = B0 ^ B1 (2)

X2 = B2 ^ (B0 & B1) (3)

X3 = B3 ^ (B0 & B1 & B2) (4)

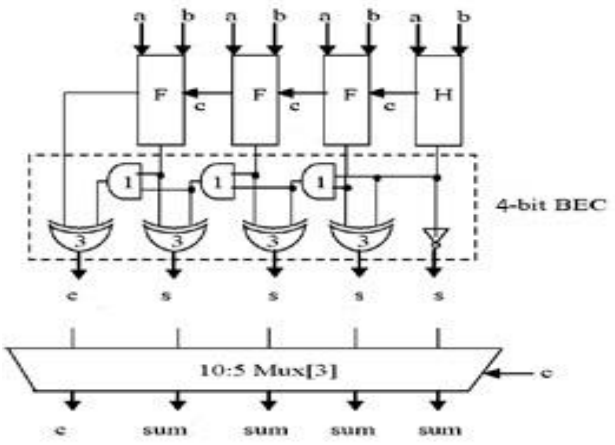

Fig.3 CSLA with BEC logic [4]

TABLE .2 Functional Table For 4-Bit BEC Logic [2]

Function Table of the 4-b BEC	
B[3:0]	**X[3:0]**
0000 0001 0010 . . 1110 1111	0001 0010 0011 . . 1111 0000

The above Figure.3 has one 4-bit RCA which has 3 FA and 1 HA for Cin = 0. Instead of another 4-bit RCA with Cin =1 a 4-bit BEC is used which adds one to the output from 4-bit RCA [2].

III. Proposed CSLA Block

In this proposed architecture the BEC logic is replaced using D-latch. In a 16-bit adder least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. Fig.4 shows the basic function of the CSLA with D-latch.

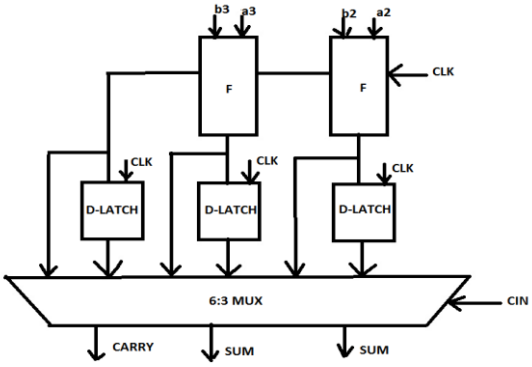

Fig.4 CSLA with D-latch

One input for 6:3 mux is D-latch output and another input for the mux is the RCA with Cin=0. This produces the two possible partial results and the mux is used to select either the D-latch output or RCA output according to the control signal Cin. This architecture further helps in the large silicon area reduction. When the clock is low a2 and b2 are added with carry value zero. The D-Latch is not enabled at this state. When the clock goes high, the addition is performed with carry value one, at this state all the Latches are enabled and store the sum and carry for carry is equal to one. According to the value of Cin, the multiplexer selected the actual sum and carry.

IV. Results and Discussion

CSLA USING D-LATCH

CLOCK :- V(40)
CARRY IN :- V(18)
INPUT :- V(4), V(36), V(41), V(45), V(55), V(59), V(59), V(63), V(75), V(79), V(83), V(87), V(101), V(105), V(109), V(113),V(117), V(2), V(37), V(42), V(46), V(56), V(60), V(64), V(76), V(80), V(84), V(88), V(102), V(106), V(110), V(114), V(118)
SUM :- V(25), V(39), V(52), V(53), V(71), V(72), V(73), V(96), V(97), V(98), V(99), V(127), V(128), V(129), V(130), V(131)
CARRY OUT :- V(132)

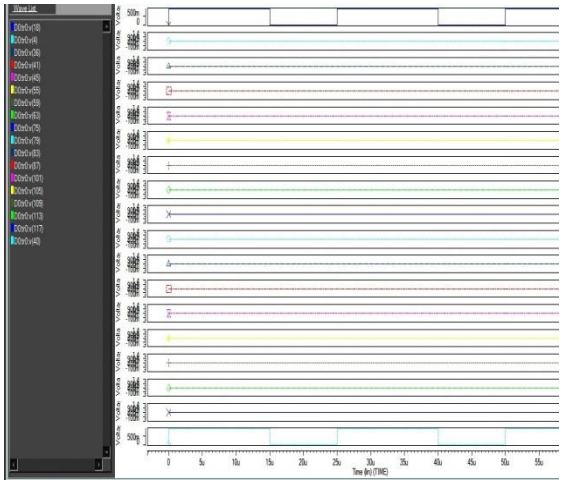

Fig.5 first 16 bit input of adder

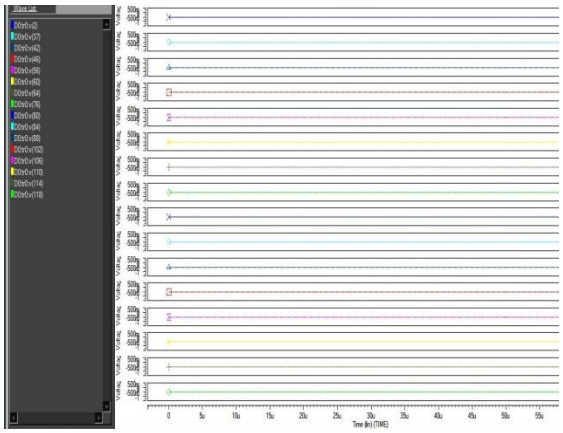

Fig. 6 second 16 bit input of adder

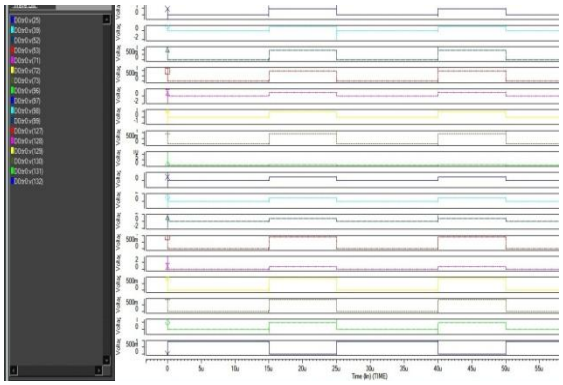

Fig.7 Output waveforms of adder

MULTIPLIER USING CSLA D-LATCH

MULTIPLIER : - V(2), V(3), V(4), V(5)

MULTIPLICAND : - V(6), V(7), V(8), V(9)

PRODUCT : - V(18), V(27), V(36),V(45),V(46),V(47), V(48), V(49)

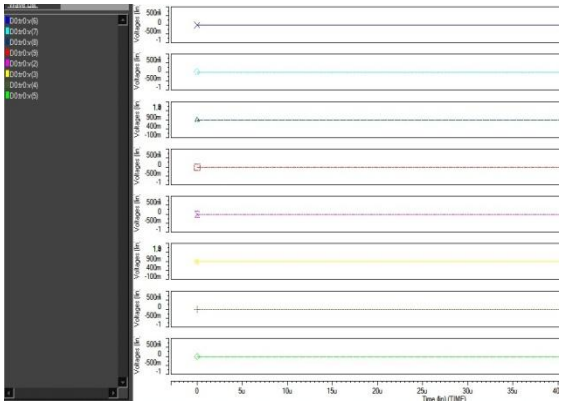

Fig.8 input waveform of multiplier

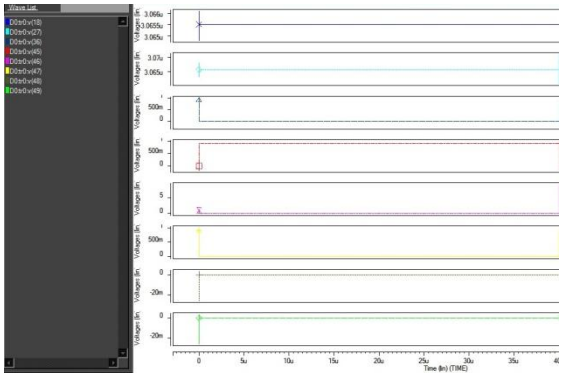

Fig.9 output waveform of multiplier

Table.3 to Table.6 illustrates power, area and delay of multipliers using existing CSLA and the proposed CSLA using 20nm FINFET and 130 nm CMOS technology. It shows that power consumption is reduced for multiplier using proposed CSLA. Similarly in multiplier using proposed CSLA area and delay is minimum.

Table.3 Area, Power And Delay Of Proposed 16 Bit CSLA Using 20nm FinFET Technology

parameters	Proposed CSLA
Power(W)	7.278e-09
No. of transistors	1,208
Delay(s)	2.34e-009
Power delay product(J)	17.03e-018

Table.4 Area, Power and Delay of 4 Bit Multiplier Using Proposed CSLA in 20nm FinFET Technology

Parameters	Multiplier using proposed CSLA
No. Of Transistors	4,832
Power	2.607e-08
Delay	2.07e-009
Power-Delay Product	5.396e-17

Table.5 Area, Power and Delay of Proposed 16 Bit CSLA Using 130nm CMOS Technology

parameters	Proposed CSLA
Power(W)	0.447e-06
No. of transistors	1,208
Delay(s)	1.36e-09
Power delay product(J)	0.608e-015

Table.6 Area, Power and Delay of Multipliers Using Proposed CSLA In 130nm CMOS Technology

Parameters	Multiplier using proposed CSLA
No. Of Transistors	1,136
Power	2.088e-06
Delay	0.382e-09
Power-Delay Product	0.747e-015

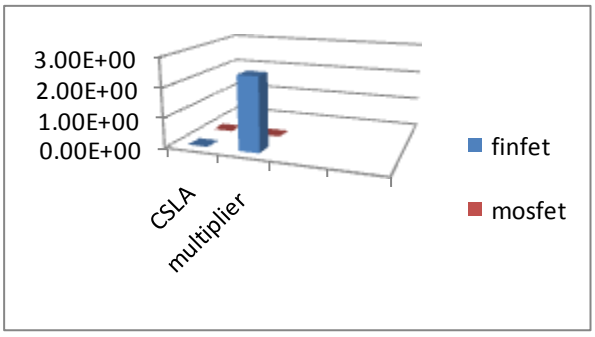

Chart 1. Power for adder and multiplier using FinFET and CMOS technology

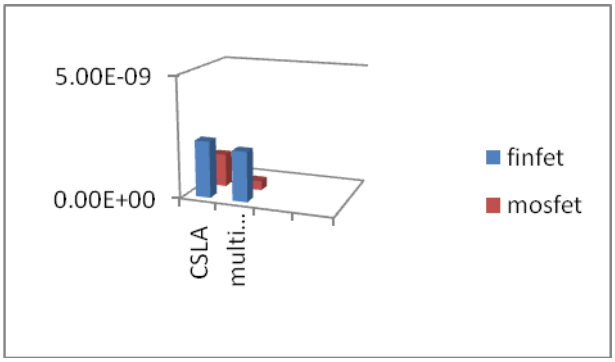

Chart 2. Delay for adder and multiplier using FinFET and CMOS technology

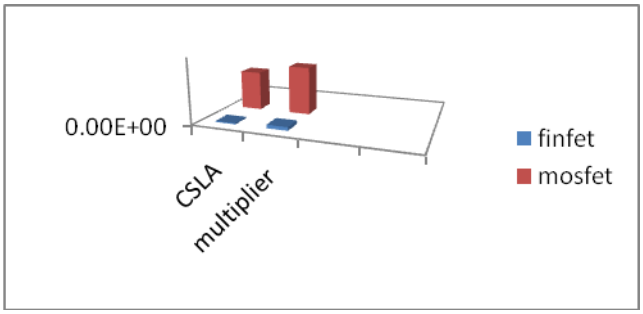

Chart 3. Power-delay for adder and multiplier using FinFET and CMOS technology

V. CONCLUSION

In this paper, multiplier is designed by carry select adder such that the proposed Carry Select-Adder is designed by single Ripple Carry Adders (RCA) and D-latches instead of using single RCA and BEC logic to reduce area and power consumption. All the circuits are simulated using HSPICE based on 20nm FinFET technology. In future, the design can be further extend for higher number of bits.

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